Claims

[c1] What is claimed is:

1.A lithography process comprising:

providing a substrate;

forming a protective layer on a surface of the substrate;

forming a patterned photoresist layer on a surface of the protective layer; and

performing a first inspection process.

[c2] 2.The process of claim 1 wherein the substrate is a semiconductor wafer, and the semiconductor wafer comprises a silicon substrate.

[c3] 3.The process of claim 2 wherein the patterned photoresist layer is used for defining the layout pattern of an ion implantation area or a shallow trench isolation (STI) on a surface of the silicon substrate.

[c4] 4.The process of claim 2 wherein the surface of the semiconductor wafer further comprises at least one deposition layer, the patterned photoresist layer is used for defining the layout pattern of the deposition layer.

[c5] 5.The process of claim 4 wherein the deposition layer comprises a silicon dioxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer, a silicon oxynitride (SiO_xN_y) layer, a polysilicon layer, or a metal layer.

[c6] 6.The process of claim 4 wherein the layout pattern comprises the pattern of a gate, a via plug, a contact plug, a dual damascence structure, a top plate of a capacitor, a bottom plate of a capacitor, a node contact, a word line, a bit line, a metal line, or a bonding pad.

[c7] 7.The process of claim 1 wherein an anti-reflection coating (ARC) is disposed underneath the bottom of the patterned photoresist layer.

[c8] 8.The process of claim 1 wherein the protective layer is a dielectric layer with a thickness of not more than 50 Å .

[c9] 9.The process of claim 8 wherein the material composition of the dielectric layer comprises silicon oxide compound or tetra-ethyl-ortho-silicate SiO_2 (TEOS-SiO

$_2$).

[c10] 10.The process of claim 8 wherein the method of forming the protective layer comprises a low pressure chemical vapor deposition (LPCVD) process or a plasma enhanced chemical vapor deposition (PECVD) process.

[c11] 11.The process of claim 1 wherein the first inspection process is an after develop inspection (ADI) process to screen the correctness of the patterned photoresist layer.

[c12] 12.The process of claim 11 wherein when the correctness of the patterned photoresist layer fulfills the spec, a normal process is performed, when the correctness of the patterned photoresist layer does not fulfill the spec, a rework process is performed.

[c13] 13.The process of claim 12 wherein the normal process comprises an etching process or an ion implantation process.

[c14] 14.The process of claim 12 wherein the rework process comprises the following steps:
performing a plasma ashing process to remove the patterned photoresist layer on the surface of the protective layer;
performing a wet cleaning process;
performing a rinsing process and a dry process;
performing a second inspection process;
reforming the patterned photoresist layer on the surface of the protective layer; and
performing a third inspection process.

[c15] 15.The process of claim 14 wherein a fluorine based solvent, an amine based solvent, or at least one chemical is utilized in the wet cleaning process to remove the photoresist layer, polymer residue, particles, and metal contamination remaining on the surface of the substrate.

[c16] 16.The process of claim 14 wherein the second inspection process is an inspection process after cleaning to inspect the cleanness of the surface of the

substrate.

[c17] 17.The process of claim 14 wherein the third inspection process is an after develop inspection (ADI) process to screen the correctness of the reformed patterned photoresist layer.

[c18] 18.A lithography process comprising:
providing a substrate, a surface of the substrate comprising at least one deposition layer;
forming a protective layer on a surface of the deposition layer;
forming a patterned photoresist layer on a surface of the protective layer to define the layout pattern of the deposition layer; and
performing a first inspection process.

[c19] 19.The process of claim 18 wherein the substrate is a semiconductor wafer, and the deposition layer comprises a silicon dioxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer, a silicon oxynitride (SiO_xN_y) layer, a polysilicon layer, or a metal layer.

[c20] 20.The process of claim 18 wherein the layout pattern comprises the pattern of a gate, a via plug, a contact plug, a dual damascence structure, a top plate of a capacitor, a bottom plate of a capacitor, a node contact, a word line, a bit line, a metal line, or a bonding pad.

[c21] 21.The process of claim 18 wherein an anti-reflection coating (ARC) is disposed underneath the bottom of the patterned photoresist layer.

[c22] 22.The process of claim 18 wherein the protective layer is dielectric layer with a thickness of not more than 50 Å .

[c23] 23.The process of claim 22 wherein the material composition of the dielectric layer comprises silicon oxide compound or tetra-ethyl-ortho-silicate SiO_2 (TEOS-SiO_2), and the method of forming the dielectric layer comprises a low pressure chemical vapor depostion (LPCVD) process or a plasma enhanced chemical vapor deposition (PECVD) process.

[c24] 24.The process of claim 18 wherein the first inspection process is an after

develop inspection (ADI) process to screen the correctness of the patterned photoresist layer.

[c25] 25.The process of claim 24 wherein when the correctness of the patterned photoresist layer fulfills the spec, an etching process is performed to transfer the layout pattern of the patterned photoresist layer to the deposition layer, when the correctness of the patterned photoresist layer does not fulfill the spec, a rework process is performed.

[c26] 26.The process of claim 25 wherein the rework process comprises the following steps:
performing a plasma ashing process to remove the patterned photoresist layer on the surface of the protective layer;
performing a wet cleaning process;
performing a rinsing process and a dry process;
performing a second inspection process;
reforming the patterned photoresist layer on the protective layer; and
performing a third inspection process.

[c27] 27.The process of claim 26 wherein a fluorine based solvent, an amine based solvent, or at least one chemical is utilized in the wet cleaning process to remove the photoresist layer, polymer residue, particles, and metal contamination remaining on the surface of the substrate.

[c28] 28.The process of claim 26 wherein the second inspection process is an inspection process after cleaning to inspect the cleanness of the surface of the substrate.

[c29] 29.The process of claim 26 wherein the third inspection process is an after develop inspection (ADI) process to screen the correctness of the reformed patterned photoresist layer.

[c30] 30.A reworkable lithography process comprising:
providing a substrate;
forming a protective layer on a surface of the deposition layer;
forming a patterned photoresist layer on a surface of the protective layer; and

performing a first after develop inspection (ADI) process to screen the correctness of the patterned photoresist layer;
wherein when the correctness of the patterned photoresist layer fulfills the spec, a normal process is performed, when the correctness of the patterned photoresist layer does not fulfill the spec, a rework process is performed by utilizing the protective layer to protect the surface of the substrate.

[c31] 31.The process of claim 30 wherein the substrate is a semiconductor wafer, and the semiconductor wafer comprises a silicon substrate.

[c32] 32.The process of claim 30 wherein the patterned photoresist layer is used for defining the layout pattern of an ion implantation area or a shallow trench isolation (STI) on a surface of the silicon substrate.

[c33] 33.The process of claim 30 wherein the surface of the semiconductor wafer further comprises at least one deposition layer, the patterned photoresist layer is used for defining the layout pattern of the deposition layer.

[c34] 34.The process of claim 33 wherein the deposition layer comprises a silicon dioxide (SiO_2) layer, a silicon nitride (Si_3N_4) layer, a silicon oxynitride (SiO_xN_y) layer, a polysilicon layer, or a metal layer.

[c35] 35.The process of claim 33 wherein the layout pattern comprises the pattern of a gate, a via plug, a contact plug, a dual damascence structure, a top plate of a capacitor, a bottom plate of a capacitor, a node contact, a word line, a bit line, a metal line, or a bonding pad.

[c36] 36.The process of claim 30 wherein an anti-reflection coating (ARC) is disposed underneath the bottom of the patterned photoresist layer.

[c37] 37.The process of claim 30 wherein the protective layer is a dielectric layer with a thickness of not more than 50 Å.

[c38] 38.The process of claim 37 wherein the material composition of the dielectric layer comprises silicon oxide compound or tetra-ethyl-ortho-silicate SiO_2 (TEOS-SiO_2), and the method of forming the dielectric layer comprises a low pressure chemical vapor depostion (LPCVD) process or a plasma enhanced

chemical vapor deposition (PECVD) process.

[c39] 39.The process of claim 30 wherein the normal process comprises an etching process or an ion implantation process.

[c40] 40.The process of claim 30 wherein the rework process comprises the following steps:

performing a plasma ashing process to remove the patterned photoresist layer on the surface of the protective layer;

performing a wet cleaning process;

performing a rinsing process and a dry process;

performing an inspection process after cleaning to inspect the cleanness of the surface of the substrate;

reforming the patterned photoresist layer on the surface of the protective layer; and

performing a second after develop inspection (ADI) process to screen the correctness of the reformed patterned photoresist layer.

[c41] 41.The process of claim 40 wherein a fluorine based solvent, an amine based solvent, or at least one chemical is utilized in the wet cleaning process to remove the photoresist layer, polymer residue, particles, and metal contamination remaining on the surface of the substrate.

[c42] 42.The process of claim 40 wherein when the correctness of the reformed patterned photoresist layer fulfills the spec, a normal process is performed, when the correctness of the reformed patterned photoresist layer does not fulfill the spec, a rework process is performed by utilizing the protective layer to protect the surface of the substrate.